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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,989	12/01/2003	Visvesvaraya A. Pentakota	TI-37261	1873

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,989	PENTAKOTA ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 6-10 and 18-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 6-10 and 18-23, there is no "second transistor" recited in previous claims to provide antecedent basis for the limitation "third or fourth transistor" as recited.

Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8-9, 12-17, 20-21 and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Flannagan (U.S Patent No. 6,031,408).

Flannagan discloses in Fig. 6 a square low clamping circuit including:

Regarding claim 1: a NMOS transistor (136) drawing a substantial amount of current from the node (121) when the voltage level at the node is greater than or equal to the upper limit (when 136 ON, and draws current on path 122. Also, the structure of the claim is met and therefore, the functional limitation is also met).

Regarding claim 2: PMOS 132 reads on a PMOS transistor which is turned on when the voltage level at the node (121) is greater than or equal to the upper limit

(when 132 ON), wherein turning on the PMOS transistor causes the NMOS transistor (136) to draw the substantial amount of current (because the structure of the claim is fully met so the functional limitation is also met).

Regarding claim 3:

a first transistor (132) designed to be turned on when the voltage level is outside of the specified range (when 132 ON); and

a current amplifier (135 and 136) drawing a substantial amount of current from the node (121) when the first transistor is turned on (132 ON), which causes the voltage level at the node (121) to be pulled to within the specified range (because the structure of the claim is fully met so the functional limitation is also met).

Regarding claim 4: elements 130-131, 122-134) read on a biasing circuit generating a bias signal to a gate terminal of the first transistor (132), wherein a voltage level of the bias signal is determined by an upper limit or a lower limit of the specified range (because the structure of the claim is fully met so the functional limitation is also met).

Regarding claim 5: wherein the first transistor (132) and the current amplifier (135-136) are contained in a high clamping circuit which clamps the voltage to the upper limit of the specified range, wherein the voltage level of the bias signal is determined by the upper limit (because the structure of the claim is fully met so the functional limitation is also met);

wherein the first transistor (132) comprises a PMOS transistor (PMOS 132), wherein a source terminal of the first transistor is connected to the node (source of

transistor 132 is connected to node 121), a drain terminal of the first transistor is connected to the current amplifier (drain terminal of transistor 132 is connected to the current amplifier 135-136), and

the current amplifier (135-136) is connected to both of the source terminal and the drain terminal of the first transistor (132).

Regarding claim 8: the current amplifier (135-136) comprises:

a third transistor (135) and a fourth transistor (136), wherein a gate terminal of the fourth transistor is connected to each of a drain terminal and a gate terminal of the third transistor (gate of transistor 136 is connected to drain and gate of transistor 135), a source terminal of each of the third transistor and the fourth transistor is connected to ground (source of transistors 135 and 136 is connected to VSS), the drain terminal of the third transistor is connected to a drain terminal of the first transistor (the drain terminal of 136 is connected to drain terminal of transistor 132), and a drain terminal of the fourth transistor is connected to a source terminal of the first transistor (drain terminal of transistor 135 is connected to source of transistor 132).

Regarding claim 9: wherein each of the third transistor and the fourth transistor comprises a NMOS transistor (135 and 136 are NMOS).

Regarding claim 12: the limitation "the first transistor comprises a NMOS transistor" is inherently seen in col. 13, lines 1-2, "the conductivity types of the transistors in square law clamps 99 or 122 may be reversed to provide analogous clamps".

Claim 13 is similarly rejected as claim 1: a high clamping circuit (Fig. 6), a NMOS transistor (136).

Claim 14 is similarly rejected as claim 2: a PMOS (132).

Claim 15 is similarly rejected as claim 3: a clamping circuit (Fig. 6), a first transistor (132), a current amplifier (135-136).

Claim 16 is similarly rejected as claim 4: biasing circuit (130-131, 133-134).

Claim 17 is similarly rejected as claim 5.

Claim 20 is similarly rejected as claim 8.

Claim 21 is similarly rejected as claim 9.

Claim 24 is similarly rejected as claim 12.

Regarding claim 25: the limitation "the device comprises a wireless base station ... an analog processor processing said external signal" is seen to define intended use. The clamping circuit of Flannagan is capable of using for wireless base state, the antenna and the analog processor as recited. **In re Tuominen, 213 USPQ 89 (CCPA 1982) & In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7, 10-11, 18-19, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flannagan as applied to claims above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Flannagan. However, this reference does not specifically show the "connection as recited in claims 6 and 10 (a gate terminal of said third transistor receiving a third bias voltage (claim 6) or (a resistor (claim 10))".

Nevertheless, these specific limitations drawn to the choice of connection is seen as design expedients dependent upon the desired results.

Therefore, it would have been obvious at the time the invention was made for one skilled in the art to realize the circuit of Flannagan using the particular connection (the gate terminal of the third transistor receiving a third bias voltage) recited in the claim 6 since this limitation drawn to a particular connection is seen as a design expedient that depends upon the desired output. For example: see Fig. 1, U.S Patent No. 5,940,322.

Regarding the resistor limitation recited in claim 10, it would have been obvious at the time the invention was made for one skilled in the art to insert the resistor connected between the source terminal of the transistor 135 and VSS in Fig. 6 of Flannagan for the purpose of providing more voltage drop and higher resistance.

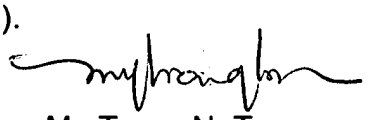
Regarding the limitation of claims 7 and 11: each of the third transistor and the second transistor comprises a NMOS transistor (135-136).

Claims 18-19 and 22-23 are similarly rejected as claims 6-7 and 10-11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

February 22, 2005